CLAIMS

What is claimed is:

1. A method for testing an integrated device comprising:

strobing a data with a strobe edge; and

measuring a setup parameter for at least one input/output circuit by pulling in the strobe edge in predetermined decrements up to a single phase of a clock..

2. The method of claim 1 measuring the setup parameter comprises providing data from a functional logic block (or FLB) within the integrated device.

3. The method of claim 2 wherein providing data comprises driving the data out through an output component of at least one input/output circuit.

4. The method of claim 1 wherein the strobe edge is on a falling edge of the clock and the data is on the rising edge of the clock.

5. A method for testing an integrated device comprising:

strobing a data with a strobe edge; and

measuring a hold parameter for at least one input/output circuit by pulling in the strobe edge in predetermined decrements up to a single phase of a clock..

6. The method of claim 5 measuring the hold parameter comprises providing data from a functional logic block (or FLB) within the integrated device.

7. The method of claim 6 wherein providing data comprises driving the data out through an output component of at least one input/output circuit.

8. The method of claim 5 wherein the strobe edge is on a falling edge of the clock and the data is on the rising edge of the clock.

9. A method for testing an integrated device comprising:

strobing a data with a strobe edge; and

measuring a setup parameter for at least one input/output circuit by pulling in the strobe edge in predetermined decrements up to a single phase of a clock,

inverting the clock after the strobe edge has been pulled in by at least the single phase of the clock; and

holding the strobe edge constant, after the strobe edge has been pulled in by at least the single phase of the clock, while pushing the data out in predetermined increments.

10. The method of claim 9 measuring the setup parameter comprises providing data from a functional logic block (or FLB) within the integrated device.

11. The method of claim 10 wherein providing data comprises driving the data out through an output component of at least one input/output circuit.

12. The method of claim 9 wherein the strobe edge is on a falling edge of the clock and the data is on the rising edge of the clock.

13. The method of claim 9 wherein pushing the data comprises pushing out a rising edge of the inverted clock.

14. A method for testing an integrated device comprising:

strobing a data with a strobe edge; and

measuring a hold parameter for at least one input/output circuit by pulling in the strobe edge in predetermined decrements up to a single phase of a clock,

inverting the clock after the strobe edge has been pulled in by at least the single phase of the clock; and

holding the strobe edge constant, after the strobe edge has been pulled in by at least the single phase of the clock, while pushing the data out in predetermined increments.

15. The method of claim 14 measuring the hold parameter comprises providing data from a functional logic block (or FLB) within the integrated device.

16. The method of claim 15 wherein providing data comprises driving the data out through an output component of at least one input/output circuit.

17. The method of claim 14 wherein the strobe edge is on a falling edge of the clock and the data is on the rising edge of the clock.

18. The method of claim 14 wherein pushing the data comprises pushing out a rising edge of the inverted clock.

19. A circuit for duty cycle clock generation comprising:

the circuit to receive an input clock;

a plurality of delay elements in a serial manner to delay an inverted version of the input clock based on a control logic; and

a multiplexer to receive a plurality of delayed and inverted versions of the input clock from the plurality of delay elements, and to forward either the input clock or one of the plurality of delayed and inverted versions of the input clock.

20. The circuit of claim 19 wherein the control logic is coupled to a phase detector, the phase detector is coupled to the input clock and one of the plurality of delay elements.

21. The circuit of claim 19 wherein the multiplexer selects the input clock in a normal operation of a integrated device and selects one of the plurality of delayed and inverted versions of the input clock in a test mode of operation of the integrated device.

22. A circuit for clock generation comprising:

a first, second and third multiplexer to receive a clock at a first input; and

the third multiplexer to receive a delayed version of the clock at a second input, the third multiplexer to select either the clock or the delayed version of the clock based at least in part on a push data enable signal.

23. The circuit of claim 22 wherein the first and second multiplexer output a data clock and

the third multiplexer output a strobe clock.

24. The circuit of claim 22 wherein the third multiplexer selects the clock if the push data enable signal is a logic zero and selects the delayed version of the clock if the push data enable signal is a logic one.

25.. An apparatus comprising:

a plurality of input/output circuit to be tested by an central control IO loopback test that:

strobes a data with a strobe edge; and

measures a setup parameter for at least one input/output circuit by pulling in the strobe edge in predetermined decrements up to a single phase of a clock.

26. The apparatus of claim 25 further comprising:

the apparatus to invert the clock after the strobe edge has been pulled in by at least the single phase of the clock; and

hold the strobe edge constant, after the strobe edge has been pulled in by at least the single phase of the clock, while pushing the data out in predetermined increments.

27. The apparatus of claim 26 wherein the apparatus is a processor.